Remarks

Claim 1 remains rejected as rendered obvious by US Pat. No. 5,991,868 to Kamiyama in view of US Pat. No. 5,740,393 to Vidwans. The Office Action maintains that the Kamiyama patent teaches a sequence of instructions including a conditional branch (Figure 6) and a branch unit (Figure 6, item 107) that selects flags read out of a memory, which are used to determine a branch condition. The Office Action further suggests that the teachings of the Kamiyama patent may be combined with the teachings of the Vidwans patent to arrive at the invention of claim 1. The Vidwans patent teaches a 2-stage multiplexer. See pages 10, last paragraph through page 11, line 6 of Paper No. 4. The Office Action maintains that it would have been obvious to one of ordinary skill in the art to combine the sequencer and branch unit taught in the Kamiyama patent with a 2-stage multiplexer with a single flag bit as output as in Vidwans. Applicant maintains that a prima facie case of obviousness is not presented in rejection of claim 1. The combination of the Kamiyama and Vidwans patents does not include "a programmable flag selection memory, a plurality of first flag selectors, each first flag selector presenting a flag from a plurality of available flags based upon contents in said flag selection memory" as claimed. Accordingly, the combination of the Kamiyama and Vidwans patents is insufficient because it does not disclose all elements and limitations of the claimed invention. See MPEP §2143.03. Accordingly, a

prima facie case of obviousness is not established. Additionally, presuming without admitting that all claim elements and limitations are disclosed in the cited references, in order to establish a prima facie case of obviousness, there must be a suggestion or teaching in the art for combining the references to arrive at the claimed invention. The fact that references can be combined does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination or provides an incentive for the combination. See MPEP §2143.01. Without the suggestion in the art to support the combination, the combination amounts to impermissible hindsight reconstruction using the claim under examination as a guide. The test for whether there is an implicit showing is what the combined teachings, knowledge of one or ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. See In re Kotzab, 217 F. 3d 1365, 55 USPQ2d 1313 (Fed Cir. 2000). In determining the differences between the prior art and the claims, the question is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. See MPEP §2141.02. The statement in support of the combination that one of ordinary skill in the art would have been motivated to combine the teachings of the Kamiyama and Vidwans patents "in order to provide a multiple stage input selector that would produce a single branching bit as a

condition for a branch to be executed" does not state particular findings in the cited art suggesting the desirability of a multiple stage input selector and resulting single branching bit, nor does it find basis for the relationship between the programmable flag selection memory and the flag selected from a plurality of available flags in the cited art. Accordingly, the rejection of claim 1 is not believed to be proper and withdrawal of the rejection is respectfully requested.

Claims 2 and 6 are rejected as rendered obvious by the combination of the Kamiyama and Vidwans patents in view of US Pat. No. 5,408,620 to Asakawa. Claims 2 and 6 are believed to be patentable for the same reasons claim 1, from which claim 2 and claim 6 depend, is believed to be patentable. Additionally, the Asakawa patent discloses a pipelined architecture for executing conditional branch instructions. As part of the disclosed process, the Asakawa patent teaches a multiple input logical AND operator in column 7, lines 7-21 and Figure 7. The disclosed logical AND operator, however, does not "accept a respective plurality of [said] branch flags"… "to create a branching bit" as claimed. Because not all elements and limitations are taught in the combination, the combination cannot render claims 2 and 6 obvious and withdrawal of the rejection is respectfully requested.

Claims 3-5 and 7-11 are rejected as rendered obvious by the combination of the Kamiyama, Vidwans patents in view of

other patents. Claims 3-5 and 7-10 are believed to be patentable for the same reasons claims 1 and 2 are believed to be patentable and withdrawal of the rejection is respectfully requested.

Applicant acknowledges allowance of claims 12-14.

Claim 15 is rejected as rendered obvious by the combination of the Kamiyama and Vidwans patents and further in view of US Pat. No. 4,742,466 to Ochiai. The combination of the Kamiyama, Vidwans and Ochiai patents does not disclose a branch unit comprising "a programmable flag selection memory, a plurality of first flag selectors, each first flag selector presenting a flag from a plurality of available flags based upon contents in said flag selection memory". The patent to Ochiai suggests that a branch address may be part of a branch instruction and does not suggest that that a compiler assigns "values for a flag selection memory" as claimed. In order for the combination to render a claim obvious, all elements and limitations must be taught or suggested by the prior art. See MPEP §2143.03. Claim 15 recites in part "each first flag selector presenting a flag from a plurality of available flags based upon contents in said flag selection memory". A compiler for converting source code including one or more conditional branch instructions must have a priori knowledge of the relationship between the available flags, the first flag selector, and the flag selection memory. None of the cited references supply teachings directed toward this relationship.

Because neither the Kamiyama, Vidwans nor Ochiai patent supplies teachings for all of the claim elements and limitations, a prima facie case of obviousness is not established and withdrawal of the rejection of claim 15 is respectfully requested.

Claims 16-18 are rejected as rendered obvious by the Kamiyama, Vidwans, Ochiai and others. Claims 16-18 are believed to be patentable for the same reasons claim 15 is believed to be patentable. Withdrawal of the rejection of claims 16-18 is respectfully requested and allowance is solicited.

If any clarifications can be made by way of telephonic interview, the Examiner is invited to contact the Undersigned.

Respectfully submitted,

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